WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory comprising:

a semiconductor substrate;

a source region provided in said semiconductor substrate;

a drain region provided in said semiconductor substrate, said source and drain regions being spaced away from each other;

an electric charge accumulating portion provided on a channel region between said source and drain regions; and

a control gate provided on said channel region, a writing operation being executed in such a way that hot electrons are generated in the vicinity of said drain region and implanted into said electric charge accumulating portion,

wherein at least said source region is provided by introducing an impurity in self-alignment with a side wall provided on a side surface of said control gate, and

an overlap of said drain region with said electric charge accumulating portion is set larger than an overlap of said source region with said electric charge accumulating portion.

2. The non-volatile semiconductor memory according to claim 1, wherein said impurity dose quantity of said source region is larger than an impurity dose quantity of said drain region.

3. The non-volatile semiconductor memory according to claim 1, wherein said electric charge accumulating portion is a floating gate provided through an insulating layer between said channel region and said control gate, and

an easing operation is performed by releasing the electrons held by said floating gate into said channel region.

4. The non-volatile semiconductor memory according to claim 1, wherein said electric charge accumulating portion is an insulating layer having a trap level therein, said insulating layer being provided between said channel region and said control gate, and

the easing operation involves neutralization of the electrons held by the trap level by injecting halls generated

in the vicinity of said drain region.

5. The non-volatile semiconductor memory according to claim 1, wherein a junction depth of said source region is larger than a junction depth of said drain region.

6. The non-volatile semiconductor memory according to claim 1, wherein said side wall is composed of a first side wall and a second side wall formed on the first side wall, and wherein said drain region is formed in self-alignment with said first side wall and said source region is formed in self-alignment with said second side wall.

7. A method of manufacturing a non-volatile semiconductor memory, comprising:

a step of providing a control gate trough an electric charge accumulating portion on a semiconductor substrate;

a step of providing a drain region by introducing an impurity outwardly of one edge of said control gate on said semiconductor substrate in self-alignment with the edge thereof;

a step of providing a side wall insulating layer on a side surface of said control gate; and

a step of providing a source region by introducing the impurity outwardly of said side wall insulating layer on said semiconductor substrate in self-alignment with said side wall insulating layer.

8. The method according to claim 7,
wherein an impurity dose quantity of said source region is set larger than an impurity dose quantity of said drain region.

9. The method according to claim 7,
wherein the impurity is introduced deeper in said source region than in said drain region.

10. A method of manufacturing a non-volatile semiconductor memory, comprising:

a step of providing a floating gate material layer through a channel insulating layer on a semiconductor substrate;

a step of providing a control gate material layer through an inter-layer insulating layer on said floating gate material layer;

a step of providing a control gate and a floating gate by sequentially patterning said control gate material layer and said floating gate material layer;

a step of providing a drain region by introducing an impurity outwardly of one edge of said control gate on said semiconductor substrate in self-alignment with the edge thereof;

a step of providing a side wall insulating layer on side surfaces of said control gate and of said floating gate; and

a step of providing a source region by introducing the impurity outwardly of said side wall insulating layer on said semiconductor substrate in self-alignment with said side wall insulating layer.

11. The method according to claim 10, wherein an impurity dose quantity of said source region is set larger than an impurity dose quantity of said drain region.

12. The method according to claim 10, wherein the impurity is introduced deeper in said source region than in said drain region.

13. A method of manufacturing a non-volatile semiconductor memory, comprising:

a step of providing a control gate trough an electric charge accumulating portion on a semiconductor substrate;

a step of providing a first side wall insulating layer on a side surface of said control gate;

a step of providing a drain region by introducing an impurity outwardly of said first side wall insulating layer on said semiconductor substrate in self-alignment with said first side wall insulating layer;

a step of providing a second side wall insulating layer

on a side surface of said first side wall insulating layer; and

a step of providing a source region by introducing the impurity outwardly of said second side wall insulating layer on said semiconductor substrate in self-alignment with said second side wall insulating layer.

14. The method according to claim 13, wherein an impurity dose quantity of said source region is set larger than an impurity dose quantity of said drain region.

15. The method according to claim 14, wherein the impurity is introduced deeper in said source region than in said drain region.

16. A method of manufacturing a non-volatile semiconductor memory, comprising:

a step of providing a floating gate material layer through a channel insulating layer on a semiconductor substrate;

a step of providing a control gate material layer through an inter-layer insulating layer on said floating gate material layer;

a step of providing a control gate and a floating gate by sequentially patterning said control gate material layer and said floating gate material layer;

a step of providing a first side wall insulating layer on side surfaces of said control gate and of said floating gate;

a step of providing a drain region by introducing an impurity outwardly of said first side wall insulating layer on said semiconductor substrate in self-alignment with said first side wall insulating layer;

a step of providing a second side wall insulating layer on a side surface of said first side wall insulating layer; and

a step of providing a source region by introducing the impurity outwardly of said second side wall insulating layer on said semiconductor substrate in self-alignment with said second side wall insulating layer.

17. A method of manufacturing a non-volatile semiconductor memory according to claim 16, wherein an impurity dose quantity of said source region is set larger than an impurity dose quantity of said drain region.

18. A method of manufacturing a non-volatile semiconductor memory according to claim 16, wherein the impurity is introduced deeper in said source region than in said drain region.

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